***POSSESION OF MOBILES IN EXAM IS UFM PRACTICE***

**Name \_\_\_\_\_\_\_\_\_\_\_\_\_\_ Enrollment No. \_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Jaypee Institute of Information Technology, Noida**

**End Semester Examination, December 2017**

**B.Tech. IIIrd Semester**

**Q4 [3+4 MARKS].** A system with 10 MHz clock uses a two level cache. The first level cache (L1) is direct–mapped, with 4KB capacity and 8 Byte blocks. The second level cache (L2) is a four way set associative, with 4MB of total capacity and 16-Byte blocks. L1 cache has a miss rate of 5%, whereas the L2 cache has a miss rate of 10%. L1 hits cause no stalls with access time of 1 clock cycle. The L2 hit time is 10 cycles. Main memory access time is 100 cycles. There is a 64-bit bus between memory and L2 cache, and between L1 and L2.

1. How many bits are used for line/set address for each cache?
2. What is the average memory access time for any instruction?

**Q6 [6 MARKS].** A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement X = (S – R \* (P + Q))/T is given below. The values of variables P, Q, R, S and T are available in the registers R0, R1, R2, R3 and R4 respectively, before the execution of the instruction sequence.

ADD R5, R0, R1; R5🡨 R0 + R1

MUL R6, R2, R5; R6🡨R2\* R5

SUB R5, R3, R6; R5🡨R3 – R6

DIV R6, R5, R4; R6🡨R5/ R4

STORE R6, X; X🡨R6

The IF, ID and WB stages take 1 clock cycle each, and the EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. Find the number of clock cycles required to complete the sequence of instructions given above.

**T3 Paper Solution**

Q4. (3 marks each)

L1 CACHE capacity = 4KB

Line size of L1 = 8 B

No. Of Lines = 4 KB/ 8B= 29

No of bits for Line Address = 9

L2 cache capacity = 4 MB

Line Size of L2 4-way set associative Cache= 16 B

No of Sets in L2 cache = 4 MB/ (4\*16 B) = 216

No. Of bits for set address = 16

b.

Hit Ratio L1 = 0.95

Hit Ratio L2 = 0.90

L1 Access Time = 1 cc

L2 Access Time 10 cc

Memory Access Time = 100 cc

Average Memory Access Time = HitRatioL1\* AccessTimeL1 + (1- HitRatioL1)\*

(MissPenaltyL1)

Miss Penalty L1 = HitRatioL2(AccessTimeL1 +AccessTimeL2) + (1- HitRatioL2) \*( Miss PenaltyL2)

Miss Penalty L2= 1cc+ 10 cc+ 2\*100 cc; two transfer from Memory to L2

= 211 cc

Miss Penalty L1 = 0.9 \*11 + 0.1 \* 211

= 31 cc

Average Memory Access Time= 0.95 \* 1+ 0.05\* 31

= 2.5 cc

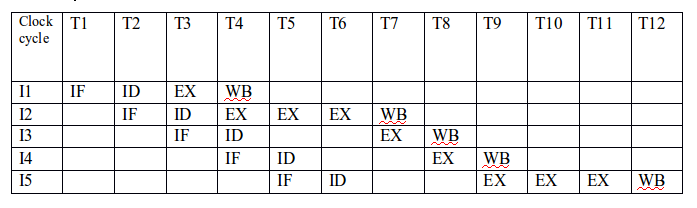
= 2.5 \*0.1 us

= 0.25 us

Q6. (6 Marks for correct 12 cc else cut 1 marks if error in forwarding EX to ID stage)

Pipelining is a technique in which the instructions are performed in parallel by executing different phases of the instructions. Generally, if two operations are performed in which second operation has dependent operands on first then, the second should not fetch operands until the first one executes as it will otherwise fetch incorrect operands. Hence, stalls are created. Now to overcome this, operand forwarding technique was introduced in which there is an interface through which the operand results are transferred. So, even if the incorrect operands were fetch during the fetch operations during the execution phase the incorrect operands are replaced by the  
correct operands.

Thus, in the given question, though MUL is dependent on ADD due to R5,SUB is dependent on MUL due to R6 DIV is dependent on SUB and STORE dependent on DIV still we can perform Instruction fetch and decode operations in the pipelined processor.



Where,  
IF-instruction fetch  
ID-instruction decode  
EX-execute  
WB-write back  
As shown in the table 12 clock cycles will be taken to perform the given instructions.